ABSTRACT OF THE DISCLOSURE

A memory architecture allows for use of non-addressable NAND memory to be used as boot memory in digital processing systems. NAND memory, which is typically of lower cost and higher density, may displace all memory in processor systems, as particularly useful in low-power processor implementations. During commencement of a boot sequence, a preselected address is provided to a NAND flash memory. This preselected address coincides with that expected by a processor unit during commencement of a boot sequence. Upon completion of a selected duration, the NAND flash increments to a next, sequential memory location and thus outputs a sequence of instructions on its data lines. The data lines of the NAND flash memory are provided as input data lines to a processor unit. The processor unit, during a boot sequence, fetches subsequent boot instructions at a timing that coincides with that which is output from the NAND flash memory.